WE CLAIM:

1. An integrated circuit fabricated in semiconductor material of a first conductivity type, said circuit having at the surface at least one lateral MOS transistor surrounded by an electrical isolation region, comprising:

a source and a drain, each having at the surface a region of the opposite conductivity type extending to the centrally located gate, defining the active area of said transistor;

a well of opposite conductivity type surrounding said source and drain, extending from said surface deep into said semiconductor material of said first conductivity type;

a semiconductor region within said semiconductor material of said first conductivity type surrounded by said well, said semiconductor region having a resistivity higher than the remainder of said semiconductor material; and

a layer of said opposite conductivity type buried in said semiconductor region;

said layer extending laterally to said wells, thereby electrically isolating the near-surface portion of said semiconductor region from the remainder of said semiconductor material, and enabling said MOS transistor to operate as an electrically isolated high-voltage I/O transistor for circuit noise reduction, while having low drain junction capacitance;

said layer extending vertically deeper from said surface than said electrical isolation region,

thereby enabling a separate contact to said electrically isolated near-surface portion of said semiconductor region.

2. The circuit according to Claim 1 wherein said semiconductor material is selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material used in integrated circuit fabrication.

3. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type is made of p-type silicon in the resistivity range from about 1 to 50 Ωcm, and said source, drain, wells, and buried layer are made of n-type silicon.

4. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type is a semiconductor epitaxial layer.

5. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type has a dopant species selected from a group consisting of boron, aluminum, gallium, and indium, while said source, drain, their extensions, and said buried layer have a dopant species selected from a group consisting of arsenic, phosphorus, antimony, and bismuth.

6. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type is made of n-type silicon in the resistivity range from about 5 to 50 Ωcm, and said source, drain, and their extensions are made of p-type silicon.

7. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type has a dopant species selected from a group consisting of

arsenic, phosphorus, antimony, bismuth, and lithium, while said source, drain, their extensions, and said buried layer have a dopant species selected from a group consisting of boron, aluminum, gallium, indium, and lithium.

8. An integrated circuit fabricated in semiconductor material of a first conductivity type, said circuit having at the surface at least one lateral MOS transistor surrounded by an electrical isolation region, comprising:

a source and a drain, each having at the surface a region of the opposite conductivity type extending to the centrally located gate, defining the active area of said transistor;

a well of opposite conductivity type surrounding said source and drain, extending from said surface deep into said semiconductor material of said first conductivity type;

a semiconductor region within said semiconductor material of said first conductivity type surrounded by said well, said semiconductor region having a resistivity higher than the remainder of said semiconductor material; and

a layer of said opposite conductivity type buried in said semiconductor region;

said layer extending laterally to said wells, thereby electrically isolating the near-surface portion of said semiconductor region from the remainder of said semiconductor material, and enabling said MOS transistor to operate as an electrically isolated high-voltage I/O transistor for circuit noise reduction, while having low

drain junction capacitance;

said layer extending vertically from said surface not as deep as said electrical isolation region, thereby enabling contacts to said electrically isolated near-surface portion of said semiconductor region in the shape of body-tied source or of angular-structured gate.

9. The circuit according to Claim 8 wherein said body-tied source is configured to provide a dual-function contact region to said MOS transistor source, and to said electrically isolated near-surface portion of said semiconductor region.

10. The circuit according to Claim 8 wherein said angular-structured gate of said MOS transistor is configured to include an H-shape or a T-shape such that its directly adjacent regions provide contacts to said source, drain, and near-surface portion of said semiconductor region.

11. A method of fabricating a buried n-type layer connecting two n-wells in a p-type semiconductor region, electrically isolating the near-surface p-type semiconductor portion suitable for fabricating a high-voltage I/O nMOS transistor, comprising the steps of:

depositing a photoresist layer over the surface of said p-type semiconductor region, and opening a window in said layer, exposing the surface area between said n-wells;

implanting, at low energy, n-doping ions through said window, creating shallow n-doped layers under said surface, suitable as extended source and drain of said transistor; and

implanting, at high energy and high dose, n-doping

ions into said p-type semiconductor through said window, creating a deep region having a net n-type doping between, and continuous with, said n-wells, and further creating a near-surface p-region having a doping concentration lower than that of the remainder of said p-type semiconductor region.

12. A method of fabricating an electrically isolated high-voltage I/O nMOS transistor in the surface of p-type semiconductor material, comprising the steps of:

forming two nested pairs of non-conductive electrical isolation regions into said p-type semiconductor material, the inner pair defining the lateral boundaries of said nMOS transistor active area, and the outer pair defining the area between n-wells;

implanting p-doping or n-doping ions to adjust the background doping level of the sub-surface region of said p-type semiconductor material;

forming n-wells into said adjusted p-type semiconductor material;

depositing over said surface a layer of insulating material suitable as gate dielectric, covering said transistor area;

depositing a layer of poly-silicon or other conductive material onto said insulating layer;

protecting a portion of said poly-silicon and etching the remainder thereof, defining the gate area of said transistor;

depositing a first photoresist layer and opening a window therein, exposing the surface of said area between said outer isolation regions;

implanting, at low energy, n-doping ions into said exposed surface area, creating shallow n-doped layers under said surface, suitable as extended source and drain of said transistor;

implanting, at high energy and high dose, n-doping ions into said exposed surface area, creating a deep region under said surface having a net n-type doping between, and continuous with, said n-wells, and further creating a p-region having a doping concentration lower than that of the remainder of said adjusted p-type region;

removing said first photoresist layer;

depositing conformal insulating layers of an insulator, such as silicon nitride or silicon dioxide, over said surface and directional plasma etching said insulating layers so that only side walls around the poly-silicon gate remain;

depositing a second photoresist layer and opening a window therein, exposing the surface of said area between said outer isolation regions;

implanting, at medium energy, n-doping ions into said exposed surface area, creating an n-doped region that extends to a medium depth under said surface, suitable as deep source and drain of said transistor;

removing said second photoresist layer; and

forming an electrical contact region to said p-region of lower doping concentration.

13. The method according to Claim 12 further including the process step of implanting, at high energy and low dose, p-doping ions for controlling the location and extent of said deep n-type region.

14. The method according to Claim 12 further including the process step of forming a p+-region as said electrical contact region to said p-region of lower doping concentration, said p+-region located close to, but electrically isolated from, the source of said nMOS transistor.

15. The method according to Claim 12 further including the process step of forming a body-tied source providing a dual-function contact region to said nMOS transistor source and to said electrically isolated near-surface portion of said semiconductor region.

16. The method according to Claim 12 further including the process step of forming an angular-structured gate, configured to include an H-shape or a T-shape such that its directly adjacent regions provide contacts to said source, drain, and near-surface portion of said semiconductor region.

17. The method according to Claim 12 wherein the thickness of said first photoresist layer is larger than a thickness solely required to block said low-energy ion implant.

18. The method according to Claim 12 further comprising the step of annealing said high energy implant at elevated temperature.

19. The method according to Claim 12 comprising the modified process step of implanting said n-doping ions at high energy after said process step of implanting said n-doping ions at medium energy.

20. The method according to Claim 12 wherein said p-type semiconductor has a peak doping concentration between 4 · 10E17 and 1 · 10E18 cm-3 after said background doping adjustment implant.

21. The method according to Claim 12 wherein said implanting of low energy ions comprises ions having an energy suitable for creating the junction at a depth between 10 and 50 nm, and a peak concentration from about 5 · 10E17 to 5 · 10E20 cm-3.

22. The method according to Claim 12 wherein said implanting of medium energy ions comprises ions having an energy suitable for creating the junction at a depth between 50 and 200 nm, and a peak concentration from about 5 · 10E19 to 5 · 10E20 cm-3.

23. The method according to Claim 12 wherein said implanting of high energy ions comprises ions selected in the energy range from about 400 to 700 keV such that the peak concentration is at a different depth than that of the p-type semiconductor, and in the dose range of about 8 · E12 to 8 · 10E13 cm-2 to overcompensate the p-type semiconductor doping and to create a region of the opposite conductivity type at a depth of more than 200 nm.

24. The method according to Claim 12 wherein said net p-type doping of low concentration comprises a peak concentration of about 1 to 6 E17 cm-3 below the p-n junctions of said transistor's deep source and drain regions.

25. A method of fabricating a buried p-type layer connecting two p-wells in an n-type semiconductor region, electrically isolating the near-surface n-type semiconductor portion suitable for fabricating a high-voltage I/O pMOS transistor, comprising the steps of:

depositing a photoresist layer over the surface of said n-type semiconductor region, and opening a window in said layer, exposing the surface area

between said p-wells;

implanting, at low energy, p-doping ions through said window, creating shallow p-doped layers under said surface, suitable as extended source and drain of said transistor; and

implanting, at high energy and high dose, p-doping ions into said n-type semiconductor through said window, creating a deep region having a net p-type doping between, and continuous with, said p-wells, and further creating a near-surface n-region having a doping concentration lower than that of the remainder of said n-type semiconductor region.

26. A method of fabricating an electrically isolated high-voltage I/O pMOS transistor in the surface of n-type semiconductor material, comprising the steps of:

forming two nested pairs of non-conductive electrical isolation regions into said n-type semiconductor material, the inner pair defining the lateral boundaries of said pMOS transistor active area, and the outer pair defining the area between p-wells;

implanting n-doping or p-doping ions to adjust the background doping level of the sub-surface region of said n-type semiconductor material;

forming said p-wells into said adjusted n-type semiconductor material;

depositing over said surface a layer of insulating material suitable as gate dielectric, covering said transistor area;

depositing a layer of poly-silicon or other conductive material onto said insulating layer;

protecting a portion of said poly-silicon and etching the remainder thereof, defining the gate area of said transistor;

depositing a first photoresist layer and opening a window therein, exposing the surface of said area between said outer isolation regions;

implanting, at low energy, p-doping ions into said exposed surface area, creating shallow p-doped layers under said surface, suitable as extended source and drain of said transistor;

implanting, at high energy and high dose, p-doping ions into said exposed surface area, creating a deep region under said surface having a net p-type doping between, and continuous with, said p-wells, and further creating an n-region having a doping concentration lower than that of the remainder of said adjusted n-type region;

removing said first photoresist layer;

depositing conformal insulating layers of an insulator, such as silicon nitride or silicon dioxide, over said surface and directional plasma etching said insulating layers so that only side walls around the poly-silicon gate remain;

depositing a second photoresist layer and opening a window therein, exposing the surface of said area between outer isolation regions;

implanting, at medium energy, p-doping ions into said exposed surface area, creating a p-doped region that extends to a medium depth under said surface, suitable as deep source and drain of said transistor;

removing said second photoresist layer; and

forming an electrical contact region to said n-region of lower doping concentration.

27. The method according to Claim 26 further including the process step of implanting, and high energy and low dose, n-doping ions for controlling the location and extent of said deep p-type region.

28. The method according to Claim 26 further including the process step of forming a n+-region as said electrical contact region to said n-region of lower doping concentration, said n+-region located close to, but electrically isolated from, the source of said pMOS transistor.

29. The method according to Claim 26 further including the process step of forming a body-tied source providing a dual-function contact region to said pMOS transistor source and to said electrically isolated near-surface portion of said semiconductor region.

30. The method according to Claim 26 further including the process step of forming an angular-structured gate, configured to include an H-shape or a T-shape such that its directly adjacent regions provide contacts to said source, drain, and near-surface portion of said semiconductor region.

31. The method according to Claim 26 comprising the modified process step of implanting said p-doping ions at high energy after said process step of implanting said p-doping ions at medium energy.

32. The method according to Claim 26 wherein said n-type semiconductor has a peak doping concentration between 4 · 10E17 and 1 · 10E18 cm-3 after said background doping adjustment implant.

33. The method according to Claim 26 wherein said

implanting of low energy ions comprises ions having an energy suitable for creating the junction at a depth between 10 and 50 nm, and a peak concentration from about 5 · 10E17 to 5 · 10E20 cm-3.

34. The method according to Claim 26 wherein said implanting of medium energy ions comprises ions having an energy suitable for creating the junction at a depth between 50 and 200 nm, and a peak concentration from about 5 · 10E19 to 5 · 10E20 cm-3.

35. The method according to Claim 26 wherein said implanting of high energy ions comprises ions selected in the energy range from about 400 to 700 keV such that the peak concentration is at a different depth than that of the n-type semiconductor, and in the dose range of about 8 · 10E12 to 8 · 10E13 cm-2 to overcompensate the n-type semiconductor doping and to create a region of the opposite conductivity type at a depth of more than 200 nm.